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MAY 15 2003

In re Application of : DECISION ON PETITION
Allen Yen et al. : UNDER 37 C.F.R. §1.144
Serial No.: 09/653,295 :
Filed: August 31, 2000 :
For: STACKED STRUCTURE FOR PARALLEL :
CAPACITORS AND METHOD OF :
FABRICATION :
:

This is a decision on the Petition under 37 CFR 1.144, filed on January 9, 2003, requesting withdrawal of the restriction requirement between product and process claims set forth in the letter of October 24, 2001.

The Petition is DENIED.

Petitioner asserts that the restriction requirement is in error because the process identified by the examiner as capable of making the product of claims 1 through 6 is not materially different from the process of claims 7 through 10, and it is not apparent that there exists any process to make the product of Group I, claims 1 through 6, which differs materially from the process of Group II (claims 7 through 10). Accordingly, the restriction requirement should be reversed.

M.P.E.P. § 803 states in pertinent part:

Under the statute an application may properly be required to be restricted to one of two or more claimed inventions only if they are able to support separate patents and they are either independent (MPEP § 806.04 - § 806.04(I) or distinct (MPEP § 806.05 - § 806.05(1)).

If the search and examination of an entire application can be made without serious burden, the examiner must examine it on the merits, even though it includes claims to independent or distinct inventions.

M.P.E.P. § 806.01 states in pertinent part:

Where two or more related inventions are being claimed, the principal question to be determined in connection with a requirement to restrict or a rejection on the ground of double patenting is whether or not the inventions as claimed are distinct. If they are distinct, restriction may be proper.

M.P.E.P. § 806.05(f) states in pertinent part:

A process of making and a product made by the process can be shown to be distinct inventions if either or both of the following can be shown: (A) that the process as claimed is not an obvious process of making the product and the process as claimed can be used to make other and different products; or (B) that the product as claimed can be made by another and materially different process.

Allegations of different processes or products need not be documented.

M.P.E.P. § 808.02 states in pertinent part:

Where the related inventions as claimed are shown to be distinct under the criteria of MPEP § 806.05(c) - § 806.05(I), the examiner, in order to establish reasons for insisting upon restriction, must show by appropriate explanation one of the following:

(A) Separate classification thereof: This shows that each distinct subject has attained recognition in the art as a separate subject for inventive effort, and also a separate field of search. Patents need not be cited to show separate classification.

(B) A separate status in the art when they are classifiable together:

Even though they are classified together, each subject can be shown to have formed a separate subject for inventive effort when an explanation indicates recognition of separate inventive effort by inventors. Separate status in the art may be shown by citing patents which are evidence of such separate status, and also of a separate field of search.

(C) A different field of search: Where it is necessary to search for one of the distinct subjects in places where no pertinent art to the other subject exists, a different field of search is shown, even though the two are classified together. The indicated different field of search must in fact be pertinent to the type of subject matter covered by the claims. Patents need not be cited to show different fields of search.

The restriction requirement of October 24, 2001 required Petitioner to elect for examination one of two inventions: Invention I (claims 1-6), drawn to a semiconductor device classified in class 257, subclass 306, and Invention II (claims 7-10), drawn to a method of making a semiconductor device, classified in class 438, subclass 100+. The restriction requirement was based on the examiner's determination that inventions I and II are distinct, each from the other, and the inventions have acquired a separate status in the art. Specifically, the examiner held that inventions I and II are related product and method of making the product. The examiner determines that the product and the method of making the product are patentably distinct since a materially different process involving selectively forming the conductive layer with openings built-in without the etching step could make the product of claims 1-6. The examiner concludes

Decision on Petition

that such a process is materially different from the process of claims 7-10.

A review of the instant application reveals that it contains two groups of claims. Claims 1 through 6 are directed to a semiconductor device and claim 7 through 10 are directed to a method of making a semiconductor device. The examiner determined that the two groups of claims are related as product and method of making the product but are distinct from each other. The method set forth in claim 7 includes a step of etching an opening in an upper most of the conductive layers and extending the opening through an adjoining dielectric layer to a first underlying conductor after a first insulative layer, a first and a second conductive runner and a stack of alternating conductor and dielectric layers have been formed. As indicated by the examiner on January 28, 2002, in response to the traversal of the restriction requirement, the semiconductor device of claims 1 through 6 may be formed by "selectively forming the conductive layers at desired areas instead of forming the conductive layers and then [sic] removing [sic] the unwanted portions of conductive layers by etching." As readily apparent from the examiner's reasoning, the selective deposition/forming of a conductive layer in the desired pattern would produce conductive layers with an opening formed in situ since the conductive material would not be deposited in the area of the opening. This process would not require the step of "etching an opening" as recited in claim 7 since the conductive layer is formed with a contact hole/opening already built in. Such a process is clearly materially different from the process of claims 7-10. The examiner has properly followed the guidelines set forth in MPEP 806.05(f) to establish that the semiconductor device of Group I and the method of making a semiconductor device of Group II are directed to distinct inventions.

Petitioner's assertion that the restriction requirement is improper is not deemed to be persuasive. Petitioner contends that the restriction requirement was made without any basis in fact and is completely in error. Specifically, petitioner asserts that the "mere removal of the element of a claim does not imply that the claimed process would be enabled by means other than the removed step. Furthermore, removal of a claim element broadens the claim while the deleted claim element remains within the scope of the claimed subject matter. Thus it is erroneous to assert that the mere removal of the etching step from claim 7 would result in a materially different process. Further, the examiner has not suggested any step to replace an etching step in order to fabricate the device of claim 1."

Petitioner appears to have misread the examiner's position in insisting restriction between the two groups of claims. The selective depositing/forming of the layers in the process of making the semiconductor device, as suggested by the examiner, would necessarily result in performing the forming steps that are materially different from the forming steps in claim 7 since material is not deposited in the area where the opening is located. Thus, the process of making the semiconductor device having an opening therein by selectively depositing material to form the layers as suggested by the examiner is clearly materially different from the method set forth in claim 7.

It is further asserted that "The undersigned is not aware of any technique, other than an etch step, for creating an opening (such as opening 88) in a dielectric layer formed over a conductive runner in a semiconductor device. Nor did the undersigned aware of any practical, or even

Decision on Petition

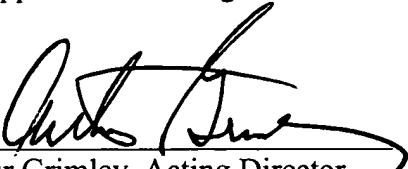
hypothetical, means (other than etching) in order to selectively form "a stack of alternating conductor and dielectric layers between the first conductive runner and the second conductive runner..." The mere fact that applicant's counsel is not aware of all the different techniques by itself is of little moment absent evidence to establish that counsel is familiar with the technology. Nevertheless, it is noted that U.S. patent No. 5,976,977 shows at least in Figs. 5 and 6 that it is known in the art to selectively depositing insulating regions 64. U.S. patent No. 6,085,413 also discloses such process step (Abstract and Fig. 1). In any event, M.P.E.P. § 806.05(f) clearly instructs the examiner that allegations of different processes or products need not be documented when asserting distinction between claims to a process of making and product made.

Although the issue of "burden in search and examination" as set forth under M.P.E.P. § 803 and § 808.02 has not been raised, the record indicates that the examiner has established that there would be a serious burden to search and examine all the claims because they are directed to divergent subject matter that requires searching in different classes of the U.S. classification system.

Since restriction requirement between the claims to the semiconductor device and to the method of making a semiconductor device is found to be proper, the petition must be denied.

Any question concerning this decision should be directed to Tom Thomas, Supervisory Patent Examiner, at (703) 308-2772.

The application is being returned to Central Files where it awaits the appeal brief.



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